REMARKS

I. Status Summary

Claims 1 and 3 are pending in the present application. Claims 1 and 3 have been amended. Therefore, upon entry of this amendment, Claims 1 and 3 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Support for the claim amendments can be found throughout the present application. For example, support for the claim amendments can be found at page 15, lines 12-37.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over EPO No. 0130381 to Auslander (hereinafter, "Auslander"), in view of Mahlke et al.; "A Comparison of Full and Partial Predicated Execution Support for ILP Processors" (hereinafter, "Mahlke"), and further in view of U.S. Patent No. 5,870,620 to Kadosumi (hereinafter, "Kadosumi"). This rejection is respectfully traversed in view of the above amendments and the below remarks.

Claim 1 recites a method for processing conditional jump instructions in a processor with pipeline computer architecture. Further, claim 1 recites loading and decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, which specifies under which conditions the instruction is actually to be executed, and a post-condition, which

specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Further, Claim 1 recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 1 recites checking the precondition, and execution of the decoded processor instruction if the precondition is fulfilled. Further, Claim 1 has been amended to recite that, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump if the post-condition is not fulfilled, and checking the corresponding flag bits, if the post-condition is fulfilled. Further, Claim 1 recites jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set. Summarily, Auslander, Mahlke and Kadosumi, alone or in combination, do not disclose, teach, or suggest each and every feature as recited by amended Claim 1.

Auslander is directed to a mechanism for fully executing a branch-on-any-bit-in-any-register instruction within one machine cycle of a host computing system. Means are provided whereby a branch decision may be made not only on a specified bit in the condition register, but on any bit in any of the general purpose registers provided in the system central processing unit (CPU). Means are also provided for saving a given configuration of the condition register in the general purpose registers for later use in subsequent branch-on-bit operations.

As described in the last response, Auslander fails to disclose, teach or suggest a post-condition as recited by Claim 1. In particular, Auslander teaches that the BI field is a pointer, not a condition which specifies a conditional jump itself, as required

by Claim 1. Accordingly, the BI field taught by Auslander cannot correspond to the post-condition as required by Claim 1.

Further, Auslander also fails to disclose, teach, or suggest the Claim 1, element (c) feature of checking flag bits corresponding to a post-condition if the post-condition is fulfilled. As such, Auslander fails to disclose, teach, or suggest the features required by element (c) of Claim 1.

Mahlke fails to overcome the significant shortcomings of Auslander to teach or suggest the claimed subject matter. The Examiner stated that Mahlke teaches an instruction containing a precondition, which specifies under which conditions the instruction is actually to be executed, and the step of the execution of the decoded processor instruction if the precondition is fulfilled. (See page 6, of the Official Action). However, Mahlke fails to disclose, teach or suggest the Claim 1, element (a) feature of a post-condition being part of a processor instruction and the Claim 1 element (c) feature of, in the case of a fulfilled precondition, checking the post-condition, and carrying out no-jump if the post-condition is not fulfilled. Further, Mahlke fails to disclose, teach or suggest the Claim 1, element (c) feature of checking flag bits corresponding to a post-condition if the post-condition is fulfilled.

Kadosumi fails to overcome the significant shortcomings of Auslander and Mahlke to disclose, teach, or suggest the claimed subject matter. The Examiner stated that Kadosumi teaches an instruction that can complete an operation, and if a logic test associated with that instruction is true, checking flag bits within the processor, and if those bits are set accordingly, branching to another instruction. (See page 4, of the Official Action.) Further, the Examiner asserts that this is completed

with only one instruction. (See page 4, of the Official Action.) However, Kadosumi fails to disclose, teach or suggest the Claim 1, element (a) feature of a post-condition which specifies that the corresponding flag bits of an arithmetic-logic unit are to be checked.

Kadosumi discloses a data driven type processor that allows alternative branch processing. Kadosumi discloses that the branch processing is done according to the addition result. (See Kadosumi, Column 13, lines 52-55.) Thus, the branch processing in Kadosumi is dependent on the addition result. Consequently, in Kadosumi, two steps have to be done sequentially. First, the addition step has to be done. Then, the second step of the branch processing can be done that is independent of this addition step. Therefore, the single step to which the Examiner refers is actually dependent upon a first addition step.

In contrast, the post-condition as recited in claim 1 is part of the processor instruction. Therefore, the branch processor is able to check very fast as to whether the post-condition is fulfilled or not, and, thus, whether a branch processing has to be done. Consequently, it is not necessary to wait for a result of another processing step such as an addition step. As a result, very complex condition settings are feasible by means of checking the precondition, the post-condition and the post-condition's corresponding flag bits of the method of claim 1. Such advantage is not reachable by a combination of Auslander, Mahlke, and Kadosumi.

Additionally, another advantage of the method recited in claim 1 is that a very fast detection for a sequential execution is provided, if the post-condition is not fulfilled. Kadosumi teaches that the processor must wait for an addition result to make a branch processing which follows in a further step of checking the corresponding valid flags.

This means a plurality of valid flags must be checked first. In contrast, the post-condition recited in claim 1 can be realized by one bit at least.

For the reasons set forth above, applicant respectfully submits that Auslander, Mahlke, and Kadosumi, alone or in combination, do not disclose, teach, or suggest each and every feature required by Claim 1. For this reason, applicant respectfully submits that Claim 1 is not obvious in view of Auslander, Mahlke, and Kadosumi. Therefore, applicant respectfully requests that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claim 3 recites an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture. Further, Claim 3 has been amended to recite an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition configured to specify under which conditions the instruction is actually executed, and a post-condition configured to specify a conditional jump is processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 3 also recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Further, Claim 3 recites that the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled. Claim 3 recites that, if the post-condition is fulfilled, checking corresponding flag bits, and if positive, driving a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction. Summarily, Auslander, Mahlke, and Kadosumi, alone or in combination, do not disclose, teach, or suggest each and every feature as recited by amended Claim 3.

Similar to Claim 1, Claim 3 recites an instruction decoder operable to decode a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Further, similar to Claim 1, Claim 3 recites that the precondition is configured to specify under which conditions the instruction is actually executed. In addition, similar to Claim 1, Claim 3 recites that the post-condition is configured to specify that a conditional jump is processed and the corresponding flag bits of an arithmetic logic unit are to be checked. Further, similar to Claim 1, Claim 3 recites that the post-condition comprises a plurality of post-condition bits that are checked in the processor. Claim 3 is similar to Claim 1 in that it recites that, if the post-condition is fulfilled, corresponding flag bits are checked. For the reasons provided above, Auslander, Mahlke, and Kadosumi fail to teach or suggest these features. Therefore, applicant respectfully submits that Claim 3 is not obvious in view of Auslander, Mahlke, and Kadosumi. Therefore, applicant respectfully requests that the rejection of Claim 3 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Summarily, the presently claimed subject matter comprises at least two main advantages compared to the cited references. First, a very fast detection for a sequential execution is provided if the post-condition is not fulfilled. Second, additional complex condition settings are feasible by means of the plurality of checked flag bits of the arithmetic-logic unit.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above amendments and remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON, TAYLOR & HUNT, P.A.

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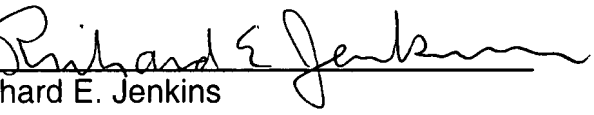
By: 

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